AM Radio Receiver

EE105 Mini-Project

Using the concepts learned in the course, we were to build amplifier and bias circuitry for an AM Radio Receiver.

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5/12/2008

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I Circuit Topology

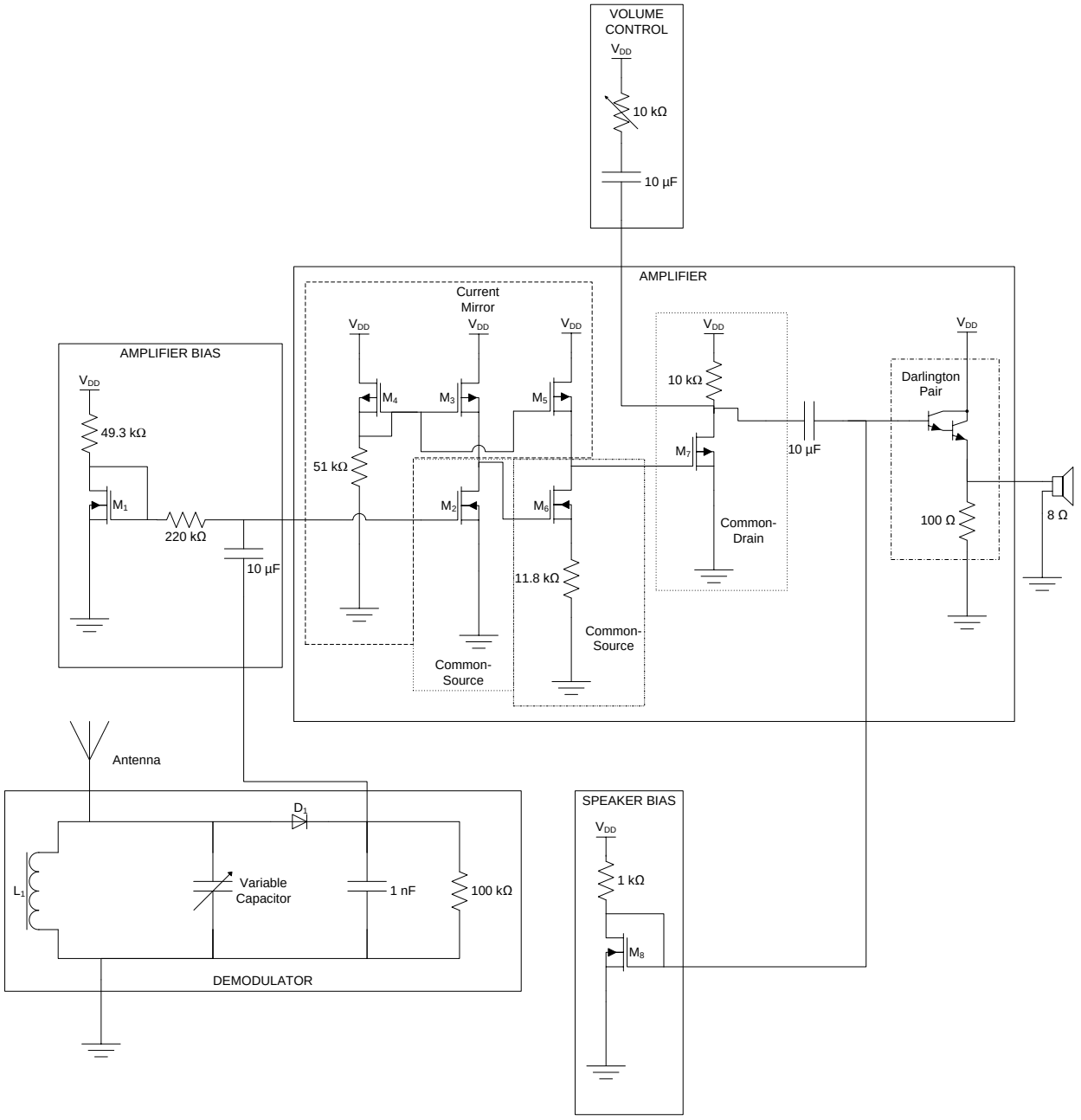

Figure 1 - Circuit Topology

II Topology Justification

Our circuit uses a two-stage common source amplifier connected to a source follower (common drain) which is connected to a Darlington Pair to amplify the signal received from our AM demodulator and drive the speaker.

MOS transistors have infinite input impedance because of the gate-bulk insulation. This implies that they have no gate currents, which is beneficial because it simplifies design and calculations. When tweaking the circuit to replicate the values for various currents or voltages, we need not worry about any parasitic effects of the base currents. It is worth noting that MOS transistors have lower gain and lower bandwidth. For our purposes, the gain of the MOS amplifiers is sufficient. Given that we are amplifying an AM signal, which operates primarily in the kilohertz range, we need not worry about the 3dB frequencies being too low and attenuating our gain.

For the amplification stage, our circuit uses a two-stage common source amplifier. The common-source amplifier was chosen because of its high gain. Given that we want an extremely high gain, we used two stages of common-source topologies. The downside of this is that the common-source amplifier has very high output impedance. Since the load to the two-stage common source amplifier is a Darlington Pair, which has a low input impedance, it is necessary to have significantly lower output impedance so that most of the output voltage is dropped over the next stage. To this end, our circuit uses a source follower output stage to buffer the output signal. This transforms the high output impedance of the common source stage to very low output impedance. The source follower (common drain) gain is near unity, so we need not worry about attenuation in the output stage. The final stage is the Darlington Pair, which consists of two BJTs with base of one connected to the input and the base of the other connected to the emitter of the first BJT (See Figure 1). The reason we use a Darlington Pair is to make sure we get a 1 V drop across our 8-Ω speaker.

The end result is an amplifier with high gain, low output impedance, and a 3dB point that is sufficiently greater than our frequencies of interest.

III Calculations

$$V_{DD} = I_{D_1} \cdot (49.3\ k\Omega + V_{GS_1})$$

$$9 = 49.3\ (0.65\ (V_{GS} - V_{Th}) + V_{GS})$$

$$|V_{GS_1}| = 0.700259\ V$$

$$I_D = -0.1684\ mA$$

M_2 is the current mirror of M_1

$M_2 \simeq M_1$ the measured values are very close

M_4:

$$9 = 51\ (0.65\ (V_{GS_4} - 0.7) + V_{GS4}$$

$$|V_{GS_4}| = 0.70025\ V$$

$$I_D = -0.1627\ mA$$

M_3 & M_5 are current mirrors of M_4

$M_3 \simeq M_5 \simeq M_4$

M_7 & M_6 are almost identically connected to the rest of the circuit

$$V_{GS7} = V_{GS6} = V_{DD} - 1.9 = 9 - 1.9 = 7.1\,V$$

$$I_{D_6} = 0.65\,(7.1 - 0.7) = 4.1\,A$$

$$I_7 \cong 4.1\,A$$

$V_x = V_{BE} = V_{DD} - I_{D_7} 10k\Omega$ = results in impractical value

$$V_x = 9 - 1.25 = 7.75$$

$$I_C = I_S e^{1.25/26\,mV} = 3031$$

$$I_y = \beta I_C = 100\, I_C$$

$$R_{out} = \frac{1/g_{m_2} \;//\; 100\,\Omega}{\frac{1}{g_{m_2}} + \frac{1}{g_{m_1}} \;//\; 100\,\Omega} = 18\,\Omega$$

$$A_V = g_{m_2}\left(\frac{1}{g_{m_1}} // 100\,\Omega\right) = 36\,\Omega$$

IV Measured Values

1 Bode Magnitude and Phase Plots

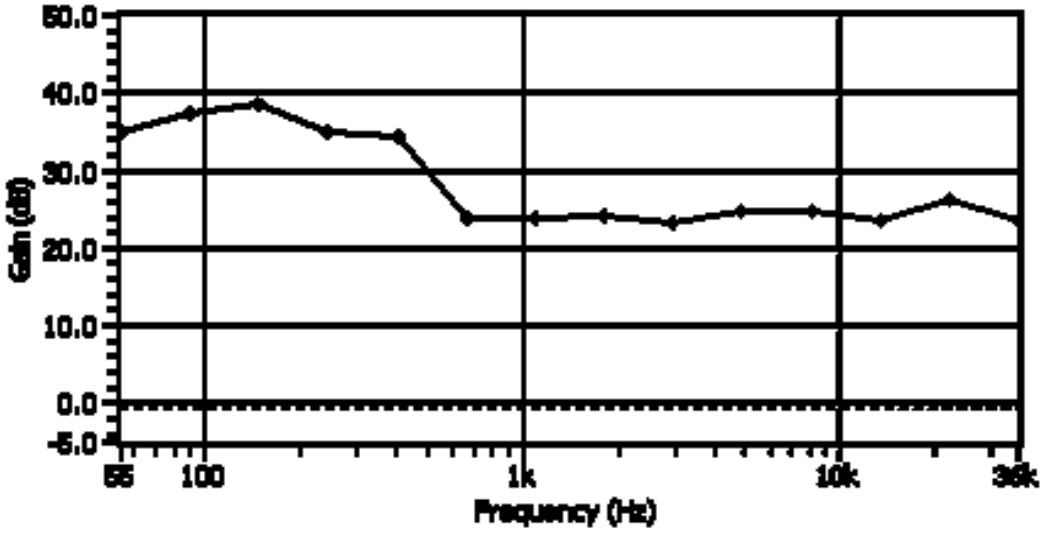

Figure 2 - Bode Magnitude Plot

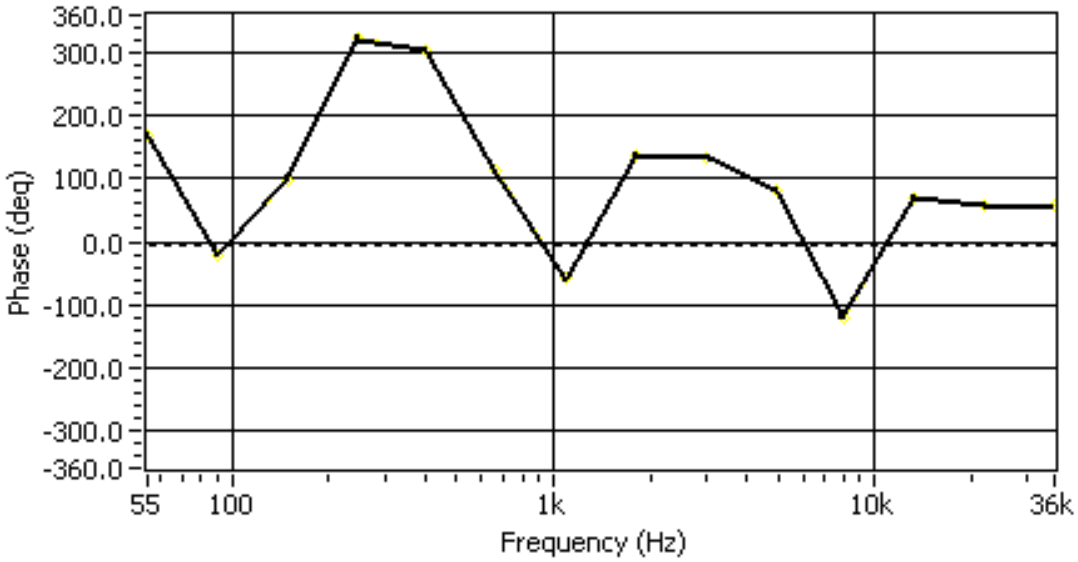

Figure 3 - Bode Phase Plot

2 Other Measured Values

Output Impedance: 3 Ω

Amplifier Bias Gate Voltage	1.3 V	Current Mirror Gate Voltage	7.26 V
Speaker Bias Gate Voltage	1.75 V		
First Stage CS Gate Voltage	1.35 V	Second Stage CS Gate Voltage	3.25 V
CD Gate Voltage	7.5 V		
Darlington Input Base Voltage	1.75 V	Darlington Output Base Voltage	1.2 V

Table 1 - Bias Voltages

Amplifier Bias Drain Current	0.153 mA	Current Mirror Current	0.142 mA
CD Drain Current	0.125 mA	Darlington Pair Collector Current	0.266 mA
Speaker Bias Drain Current	0.368 mA		

Table 2 - Bias Currents

3 Power Consumption

$$Total\ Power = V_{DD} \cdot \sum_i I_{D-i}$$
$$= 9V \times (0.153mA + (3 \times 0.142mA) + 0.125mA + 0.266mA + 7.2mA)$$
$$= \mathbf{73.53mW}$$